Resume: Uri Weiser

RESUME
URI C. WEISER

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EDUCATION & TITLES

ACM *Fellow*		2005
Distinguish *Fellow* of the Electrical Engineering Department, Technion	2004	
IEEE *Fellow*		2002
Intel *Fellow*		1996
Ph.D. Computer Science, University of Utah	1981	
M.Sc. Electrical Engineering, Technion		1975
B.Sc. Electrical Engineering, Technion		1970

INDUSTRIAL EXPERIENCE

2010 - present **We-Fi** (startup – Wi-Fi)
Senior Advisors: Strategy and solutions

2008 - present **Lucid** (startup - graphics)
Board of Advisors: Power analysis and advantages, new approach to CMP

2007 - present **NovaTrans** (startup - devices)
Senior Scientific and Technological Advisor

2007 - 2008 **Commex-Technologies** (startup – x86 chipsets)
New X86 Platform approach – I/O Data content aware chipset
CTO - Chief Technology Officer

1988 - 2006 **Intel Corporation**

2001 - 2006 **Intel Israel,** Corporate Technology Group (CTG)
Director, Streaming Media Architecture Laboratory

1999 - 2000 **Intel Austin (Texas, US),** MicroProcessor Group (MPG)
Co-Manager of Texas Development Center

1993 - 1998 **Intel Israel,** MicroProcessor Group (MPG)
Director of Computer Architecture and Planning Department, VLSI Design Center

1991 - 1992 **Intel Santa-Clara (California, US)** MicroProcessor Group (MPG)
Director of Platform Architecture Center (PAC)

1988 - 1990 **Intel Haifa (Israel), VLSI Design Center**
Manager of MicroProcessor Architecture Group

1984 - 1988 **National Semiconductor, Herzelia (Israel), VLSI Design Center**
Architecture Group **Manager**, NS32532 **design Manager**

1970 - 1984[1] **Israeli Ministry of Defense, Israel Armament Development Authority-Rafael, Haifa, (Israel)**
Technical Group Manager (Analog/Digital), System Engineer

ACADEMIC APPOINTMENTS

Technion (Haifa, Israel)

2007- present **Professor** (visiting), **Technion, Israel,** Faculty of Electrical Engineering
Research: VLSI Architecture, Memory/Cache subsystem, Data content aware platforms
Course: Computer Architecture, Architecture of VLSI systems M.Sc/Ph.D students' Thesis advisor

1982 - 2006 Adjunct associate professor. Department of Electrical Engineering

2009 - present Inter-Disciplinary Center **(Herzelia, Israel)**
Visiting Professor. Computer Science Department – Course: Advanced topic in Computer Architecture

>40 publications. 10 patents, 3 Intel's Awards, Associate Editor *IEEE Computer Architecture Letters*. Invited speaker at numerous Univ/conferences/workshops. Currently Thesis advisor of 4 M.Sc/Ph.D students
Personal Interests: Diving; certified diver 2 stars, 1977, Flying:(private fixed-wing pilot license "group A - VFR" 1997, helicopter training (R22) solo 9/2009), Sailing (Israeli certified skipper, 2006), hiking, skiing, traveling, teaching. Interested in art, especially performing arts: modern dance, classical music, jazz, theater.

[1] 1978 - 1981 Sabbatical for Ph.D studies and completion

RESUME (DETAILED)

EDUCATION & TITLES

- ACM *Fellow*, 2005

"For leadership in superscalar and multimedia architectures"

- EE Distinguish *Fellow*, Electrical Engineering Department, Technion, 2004

"For his pioneering R&D activities in the area of computers and microprocessors architecture promoted under his leadership at RAFAEL, National Semiconductors and Intel. For his technological breakthroughs in the development of NS32532 microprocessor, Intel Pentium Definition, the Intel MMX technology and the invention of the Trace Cache"

- IEEE *Fellow*, 2002

"For Contributions to Computer Architecture"

- IEEE Senior member, 1999

- Intel *Fellow*, 1996

Intel's 12th Fellow: for the invention of the Pentium processor and MMX Technology.

- Ph.D Degree, 1981

Computer Science Department, University of Utah S.L.C. Utah
Areas of Interest: Signal Processing; Digital Hardware; VLSI Computer Architecture
Thesis Title: *"Mathematical and Graphical Tools for the Creation of Computational Arrays"*
Advisor: Professor Alan L. Davis

- **M.Sc. Degree, 1975**

Department of Electrical Engineering, Technion, Israel Institute of Technology, Haifa, Israel
Specialization: Analog Circuits, Electronics; Circuit Theory; Control; Signal Processing
Thesis Title: *"A Logarithmic Preamplifier for Laser Signal Detection"*
Advisors: Professor Arie F. Arbel, Amnon Adin

- **B.Sc. Degree, 1970**

Department of Electrical Engineering, Technion, Israel Institute of Technology, Haifa, Israel

INDUSTRIAL EXPERIENCE

2007 - present: Lucid (graphics startup)

- *Board of Advisors: Power analysis and solutions*

2007 - present: NovaTrans (Basic Component startup)

- *Senior Scientific and Technological Advisor*

2007 - 2008: Commex-Technologies (Chip-Set startup)

- ***CTO- Chief Technology Officer (part time)*** *(2007-2008)**;***
  An innovative Platform Efficient Solution (IP protected). "Data Dependent Platform's Traffic Controller"

1988 - 2006: Intel Corporation

- ***Intel, Israel (2002 - 2006), Petach-Tikva & Haifa, Israel***

Position: **Director, Corporate Technology Group, Israel**

Activities 2005-2006: - Accelerator Architecture research: based on application analysis. Define Streaming Media accelerator architecture to achieve high performance and performance/power figures.
- Member of Intel's Fellow nomination committee

Activities 2002-2004: - Initiated Streaming Media Architecture advanced development activity. Outcome was the Asymmetric Cluster (cores) Chip MultiProcessors (ACCMP) and Accelerators concepts: e.g. Streaming/Media Co-processors cores adjacent (on the same die) to the main host cores. This includes the application analysis, usage model, cores architecture, Microarchitecture, Interconnect scheme, and SW model.

- ***Intel, Israel (2001), Haifa & Petach-Tikva, Israel***

Position: **Director, Strategic Investments, Intel Capital.**

Activities: - Heavy lifting deals: creating a spin-off in a new technological and business domain
- Streaming Processing Initiative

- ***Intel, Texas Development Center (1999 – 2000), Austin, TX, USA***

Position: Co-Director* of Intel's Development Center (X86 high end MicroProcessor design) *(200 engineers)

Activities:
- **Established a new design center from grounds up**
- Co-lead the establishment of the Development center's Infrastructure (building, computing and communication), products (strategic planning), products Architecture and marketing, design methodologies, management structure, HR, Finance.
- Definition of the next X86 lead processor.
- **Initiated and defined a new Streaming Co-Processor Architecture**
- Intel's Fellow Nomination Committee

- ***Intel Israel, VLSI Design Center (1993 - 1998), Haifa, Israel***

Position: Director of Architecture and Planning Department (20 engineers)

Activities:
- Architecture Definition of Pentium Extensions Products **(Pentium with MMX™ Technology)**
- Driving X86 Processor's Future Products Definition, Solutions, Analysis and Strategy
- **Definition of Intel's Multimedia Architecture (MMX™ Technology)**
- Research Intel's X86 new Processor's Microarchitecture
- Led a research and definition of a new MicroArchitecture concepts
- Intel's 1977 Innovation Day – member of the nominations committee

- ***Intel Santa Clara, MicroProcessor Group (1991 - 1992), Santa Clara,CA, USA***

Position: Manager, Platform Architecture Center, MicroProcessor Group (50 engineers)

Activities: **Leading Intel's X86 future strategy**, directions and analysis.
- Intel's CPU and Cache strategies and future product roadmap
- **The group performed the initial definition of PCI™ (Peripheral Components Interface)**
- Performance analysis of MicroProcessors
- High Level Definition of Intel's Chipsets
- Intel's X86 Processor research

- ***Intel Israel, VLSI Design Center (1988 - 1990), Haifa, Israel***

Position: MicroProcessor Architecture Group Manager (8 engineers)

Activities:
- **Initiation, concept definition and feasibility studies of Intel's Pentium™ MicroProcessor**
- Defined X86 superscalar, branch predication and split Instruction and Data cache concepts
- Analysis of Performance limitation of CISC MicroProcessor
- Architecture definition of Cache Controller (C5/C8)
- Architecture definition of new i860 family MicroProcessor

1984 - 1988: National Semiconductor VLSI Center (Israel), Herzelia, Israel

- ***Position: Chief Scientist (1988)***

Activities:
- Definition of on Die (Chip) protocols, Definition of VLSI Design Methodology
- Conduct NS32532 MicroProcessor session in International Conference on Computer Design (ICCD)

- ***Position: NS32532 CPU Design Manager (1985-1987)***

Activities:
- **Manage NS32532 CPU** design (Architecture, design, circuit, layout)
- NS 32532 Project management
- NS32532 Architecture definition including Multiprocessing support
- VLSI Circuit support (Standard & special cells, clock generators, sense amplifiers), layout integration

- ***Position: Computer Architecture Group Manager (1984)***

Activities:
- Performance evaluation
- Multiplication, division algorithms for floating point arithmetic
- Multicomputer research (in conjunction with the Technion)

1983 (Summer): Laboratory for Artificial Intelligence, Fairchild, Palo Alto, CA, USA

Working with Professor Alan Davis on AI Architecture

1970 - 1984[2]: Israel Armament Development Authority (RAFAEL), Israel Ministry of Defense, Haifa, Israel

- ***Position: System Engineer, 1981-1984***

Activities:
- Supervisor and advisor for the development of computer system for Command and Control
- Design for System reliability, and security (encryption)
- Project management, long-term planning

[2] 1978 - 1981 Sabbatical for Ph.D studies and completion

- ***Position: Group Manager, 1975 - 1977***

Activities: - Research in the area of Fast Signal Measurement, Sampling, Fast A/D, transient Digitizer.
- Development and integration of high-resolution measurement and data recording system combining Analog and Digital equipment.

- ***Position: Research Engineer, 1972 - 1975***

Activities: - Very fast linear feedback Amplifier Analysis and development
- Research: speed limitation of feedback amplifiers due to loop delay
- Research: fast logarithmic amplifiers

- ***Position: Group Leader (Project Manager), 1970 - 1972***

Activities: Design/Implementation of an Automatic Radio Frequency Interference (RFI) Test System (Digital and Analog)

ACADEMIC APPOINTMENTS

1974 – 1977, 1982 – 1990, 1992 – 1998, 2001 – present:
Electrical Engineering Department (part-time), Computer Science Department (part-time),
Technion, Israel Institute of Technology, Haifa, Israel

- **Professor** (visiting)
  One of the leading members of "MATRICS: Multiple AsymmeTRic Interconnected Core Systems"; an EE Technion research initiative http://www.ee.technion.ac.il/matrics/

Teaching Experience:

- Architecture of VLSI systems (EE and CS graduate course)
  Up-to-date VLSI Microarchitecture and platforms concepts and techniques
- Computer Architecture 101 (EE and CS undergraduate/graduate course)
- Electronic Instrumentation (undergraduate course)
- Advanced Design of Linear Circuits (graduate and undergraduate course, 1976)

Co-Manager/Co- Chief researcher (w/ Professor Idit Keidar) **of the EE "CMP Knowledge Center"**

- Established an infrastructure for CMP research at the Technion's EE department. The infrastructure will be used by researchers in Israel, and the center will act as a source of CMP tools and knowledge.

Graduate Students - Master/Ph.D thesis advisor (EE Technion, Haifa, Israel):

- "Efficient Systolic Array for Matrix Multiplication", *M.Sc thesis* Fabian Klass, 1986
- "End to End Communication Protocol in a MIMD Computer - Definition and Implementation as part of Independent Communication Element", *M.Sc thesis* by Ilan Zisman, 1987.
- "Point to Point Communication and Routing Protocol for a MIMD Computer - Definition and Implementation as Part of Independent Communication Element", *M.Sc thesis* by Yoram Rimoni, 1987
- "Performance Limitation of CISC Processor", *M.Sc thesis* by Alex Peleg 1991
- "Power issues of on Chip Interconnect", *M.Sc thesis*, by Nir Magen, December 2003
- "Data Trace Cache" *M.Sc thesis,* by Tomer Morad, March, 2005,
- "Streaming cache structure" *M.Sc thesis* by Dror Barash, *Dec* 2007
- "Dynamic Voltage Scaling technique in ACCMP systems" *M.Sc thesis*, by Avshalom Elyada, Apr 2007
- "Nahalal; new-cache Organization for Chip Multiprocessors", *M.Sc thesis*, by Zvika Guz, January 2008
- "Cache Organization and control for Chip Multiprocessors", *Ph.D thesis*, , by Zvika Guz, expected 2010
- "Multiple Clock and Voltage Domains for Chip Multi Processors" *M.Sc thesis* by Efi Rotem expected 2010
- "Asymmetric Cluster CMP" *Ph.D thesis*, by Tomer Morad, expected 2011
- "NUMA Memory transaction offloading" *M.Sc thesis* by Leonid Azriel, expected 2011
- "Thermal based Task Scheduling Optimization in CMP" Tomer London undergraduate-excellent-students-project, expected 2009

2002 – 2005:
School of Engineering (part time), Hebrew University (Jerusalem, Israel)

- **Adjunct Professor**
  - School of Engineering curriculum and Program

1977 - 1981: Computer Science Department, University of Utah, S.L.C., Utah, USA

- **Research Assistant** (1978, 1981)**:**
  Switching networks, Algorithms for Concurrent Environment, Mathematical Representation of Computational Arrays, Pitch Tracker using Short-Time Furrier Transform,
- **Teaching Assistant** (1977-1978)

Fall 1980: Information Sciences Institute (ISI), University of Southern California
Working with Dr. Danny Cohen, research topic: Algebra of Pipelining

PATENTS and AWARDS:

- **Y. Peleg, T. Horowitz, U. Weiser "Data path topology optimizations in computer systems"** US Patent Provisions May 2009 *aka M_3*
- **Y. Cohen, U. Weiser et al "System and Method for Routing Packets Using Tags"** US Patent Applications, May 2008, Serial No: 12/120,656
- **U. Weiser, et al: "System and Methods for Efficient Handling of Data Traffic and Processing within a Processing Device"** U.S. Patent Application July 2007. Serial No: 11/776,285, *aka Content Aware Routing (Actions)*
- **U. Weiser, et al; "A Mechanism for Enabling the Utilization of Idle OS Processors' Cycles",** United States Patent in filing, September 2005
- **U. Weiser, et al; "Branch Prediction and Resolution Apparatus for Superscalar Computer Processor",** United States Patent No. 5,606,676, Feb. 25, 1997
- **U. Weiser, et al; "Boundary Markers for Indicating the Boundary of Variable Length Instruction to Facilitate Parallel Processing of Sequential Instructions",** United States Patent No. 5,450,605, Sep. 12, 1995 *aka Bit Per Byte*
- **A. Peleg, U. Weiser; "Dynamic Flow Instruction Cache Memory Organized Around Trace Segments Independent of Virtual Address Line",** United States Patent No. 5,381,533, Jan 10, 1995 *aka Trace Cache*
- **U. Weiser, et al; "Branch Prediction and Resolution Apparatus for Superscalar Computer Processor",** United States Patent No. 5,442,756, Aug. 15, 1995
- **U. Weiser, D. Perlmutter, Y. Yaari; "Pipeline System for Executing Predicted Branch Target Instruction in a Cycle Concurrently with Execution of Branch Instruction"**, United States Patent No. 5,265,213, Nov. 23, 1993
- **U. Weiser et al; "Memory Referencing in High Performance MicroProcessors"**, U.S. Patent Application #RS51842/9115026.8, 1977?
- **Intel Achievement Award (IAA)** 1997,
  "For Innovation that Transformed MMX Technology from Concept to Reality"
- **Intel Achievement Award (IAA)** 1990,
  "For the Initiation and Development of an X86 Performance Simulator" (the Pentium Processor simulator)
- **Intel Israel Design Center, Divisional Recognition Award (IDA)** 1989**,**
  "In Recognition for Your Outstanding Achievement in Reviving the X86 Architecture by Generating the Px Product Proposal" (*the initial definition of the Pentium Processor*)

INVITED LECTURES and PANEL MEMBER:

- **"Computing dilemma: Cache and/or Threads?"** invited talk at Intel, Haifa, Israel, July 12th, 2009
- **"CMP and NUMA environments - new Computer Architecture challenges"** invited talk at University of Wisconsin, MA, June 18th, 2009
- **"Cache and/or Threads, MC vs. MT engines"** invited talk at Intel, Portland, OR, CA, June 16th, 2009

- **"Asymmetric Applications and Hardware reciprocal"** talk at UC Berkeley, CA, PARLAB, EECS, June 15th, 2009
- **"Cache and/or Threads, MC vs. MT engines"** invited talk at nVidia, Santa Clara, CA, June 12th, 2009
- **"Asymmetric Chip Multi-Core – Applications and Processors – initial thoughts"** Invited talk at the Princeton University, EE Colloquium, , NJ February 19th, 2009
- **"Asymmetric Chip Multi-Core – The future Chip Multiprocessor"** Invited talk at the Alternative Computing Day, Ben Gurion University, Beer Sheva, Israel, February 9th, 2009
- **"Asymmetric Chip Multi-Processor – Applications, Processors and OS – Initial thoughts"** Invited talk at the MultiCore Day: The challenges of today and tomorrow, Israel Ministry of Science Knowledge Center on CMP, Technion, Haifa Israel, February 3rd, 2009
- **"VLSI Processor's Architecture"** invited talk at the Technion, undergraduate enrichment lecture series Haifa, Israel, January 8th, 2009
- **"Asymmetric on die computation and Asymmetric IO services: environment and solutions"** invited talk at IBM Yorktown Heights, February 1st, 2008
- **"Content Aware Routing"** Microsoft Platform evaluation group, December 19th, 2007
- **"Decisions in Risk environment"** Invited talk and Panel member, Synopsys Executive Event, Tel Aviv, Israel, May 1st, 2007
- **"Either innovate - or go to a place nobody is"** Talk and Panel member, 2nd Innovation summit, Haifa, Israel, March 21st, 2007
- **"Symmetric vs. Asymmetric Chip Multi-Processor"** Invited talk, Universidad Politecnica de Catalunya (UPC), Barcelona, Spain, February 14th, 2007
- **"Why not Symmetric Chip MultiProcessing"** nVidia Colloquium, Santa Clara, CA. December 13th, 2006.
- **"Turning Brains into Bucks"** Panel member, Conference Steering committee, Distributed & Multi-Computing session chair, The 1st Israel Innovation Summit, Haifa Israel, April 4-5, 2006.
- **"The Intel Platform Revolution"** Panel discussion**,** Intel's Fellow Forum**;** Napa, CA, September 21, 2005
- **"Continuing Moore's law: The Special-Purpose Path: From Programmable Engines to Fixed Function Accelerators"** Intel's Fellow Forum**;** Napa, CA, September 21, 2005
- **"Future direction in Microprocessors" Keynote Speaker, "Technology in Motion"** Intel's Mobility Vision**;** Tel-Aviv, Israel, May 30, 2005
- **"The road not taken, or future direction in Microprocessor design", Intel's Mobility Group,** Design Enrichment Seminar, Intel Haifa, May 22, 2005
- **"Is it the end of the Hard-Ware complexity era in Microprocessors" Keynote Speaker,** Intel's EMEA 10th Academic Forum; Gdansk, Poland, May 19, 2005
- **"Microprocessors: Bypass the power wall (at least for a while)" Plenary Speaker,** ICECS, **11th IEEE International Conference on Electronics, Circuits and Systems,** Tel Aviv, Israel, December 14, 2004
- **"Asymmetric Cluster Chip MultiProcessing (ACCMP)" Special Colloquium, Department of Electrical engineering,** Tel Aviv University; November 22, 2004
- **"From Individual Contributor to Intel Fellow - a story at a glance" Invited talk, Intel Petach Tikva, Senior Technology Contributors Program - Israel,** Kefar Vitkin, Israel; November 1, 2004, **also: Intel FAB8/FAB18,** Jerusalem; June 28, 2005
- **"The Road not Taken" Invited talk, 1st Technical Leadership Innovation Conference at Intel - Israel,** Tel Aviv, Israel; October 17, 2004
- **"The real life limitations of converged core" Panel member, Intel's 3st MicroArchitecture Forum,** Barcelona, Spain, June 29, 2004
- **"Streaming Facility for DLite IA32 Media - Optimized Light Weight Cores",** Intel's 3st MicroArchitecture Forum**, Barcelona, Spain,** June 28, 2004 (Co-Author)
- **"Microprocessors: Extend Moore's performance law within limited power envelop" Invited talk,** Intel Bangalore, India, Innovation day, May 5, 2004
- **"Microprocessor: Bypass the power wall" Invited talk,** Intel's EMEA 9th Academic Forum**;** Barcelona, Spain, April 21, 2004
- **"Media extension to X86 family" Panel member,** Intel's Senior Technical staff meeting**,** November 19, 2003 **- "Where should we go with Microarchitecture?" Panel member,** Intel's 2nd MicroArchitecture Forum**,** Santa Cruz, US, June 12, 2003

- **"Microprocessors: Is Moore's law ended? Do we hit a wall?" Invited talk, Intel's** EMEA 8th Academic Forum**;** Berlin, Germany, April 28, 2003
- **"Microprocessors: Will Moore's law continue?", Invited talk,** Intel's Symposium **Performance Verification Technologies,** Haifa, Technion Israel, June 25, 2002
- **"PC Streaming Processing",** Intel's 1st MicroArchitecture Forum, Mt Hood, Oregon, May 23, 2002
- **" Innovations in VLSI Architecture", Invited talk,** Universidad Politecnica de Catalunya **(UPC),** Barcelona, Spain, April 17, 2002
- **"The Yearn for Specialized MIPS, a Proposed Solution", Invited talk,** Universidad Politecnica de Catalunya **(UPC),** Barcelona, Spain, April 16, 2002
- **"Innovations in Computer Architecture", Invited talk,** EMEA 6th Intel Academic Forum**;** Istanbul, Turkey, September 6, 2001
- **"MicroProcessor Architecture – How to reach the next Performance Step?", Invited talk,** Intel's Symposium on **Logic and Validation Technologies;** Haifa, Technion Israel, July 24, 2001
- **"Specialized MIPS and Solutions" Invited talk,** EMEA 5th Intel Academic Forum**;** Prague, September 13, 2000 **also at Intel's Fellow Forum;** Portland, September 26, 2000
- **"VLSI: Is it all about Integration and Performance? Trends and Directions"** Invited talk, MIT VLSI **Colloquium; November 2, 1999. also at** Pasadena, Caltech**; January 12, 2000.** Austin, University of Texas, ECE Colloquium; Boston, February 15, 2000, **also at the** Technion **EE Merlin Memorial Lecture,** Haifa, April 5, 2001
- **"VLSI MicroProcessor Architecture – Integration/performance Trends and Future Directions", Invited talk, ICCD Conference:** Austin, Texas, October 12, 1999
- **"MicroProcessor Architecture – What is next?" Invited talk, Intel's Design Technology Conference:** Santa Clara, CA, June 18, 1999
- **"MicroProcessor Architecture, Trends and Directions", Intel Distinguished Lectures in Europe;** Cambridge, UK, July 16, 1998, **also at ILA (Israel Science Association) Conference,** Haifa, Israel, June 27, 1998
- **"Idea, Tradeoffs, Driving and Performance of Intel's MMX™ Technology", British Petroleum Innovation Colloquium;** London, UK, July 29, 1997
- **Panel member: "Synchronous vs. Asynchronous Design", International Solid State and Circuit Conference, ISSCC97,** San Francisco, CA, February 8, 1997
- **Invited Lecture: "Future Directions in MicroProcessor Design",**
  - **University of Utah** (February 1996),
  - **CALTEC; California Institute of Technology** (February 1996)**,**
  - **Stanford** (March 1996)**,**
  - **Technion** (June 1996)**,**
  - **UCLA** (February 1997)**,**

    part of Intel's 1996 Distinguished Lectures in Technology Series.
- **Panel member: "Enhancement Host CPU Architecture for Multimedia", MicroProcessor Forum Conference,** San Jose, CA, October 1996
- **"Future Trends in MicroProcessor Architecture Design", International Symposium on Advanced Research In Asynchronous Circuit and Systems,** Aizu, Japan, March 1996 (lecture was given by Shai Rotem, due to unavailability of the lecturer)
- **"A New VLSI Design Methodology" Workshop on VLSI (NSF and IL-NCRD),** Tiberias, Israel, May 1987

PROFESSIONAL ACTIVITIES: JOURNALS, CONFERENCES and COMMITTEES ACTIVITIES:

- **37th Annual International Symposium on Computer Architecture (ISCA) 2010;** Program Chairman**;** Saint-Malo (France) **to be held in June 20th-23rd, 2010**
- **High Performance Computer Architecture (HPCA) conference; SLC, UT, Feb-2008**, Member of the Program Committee, session chair
- **International Symposium on Computer Architecture (ISCA);** Austin**- 2009**[1], Beijing**-2008**[1,3]**,** Madison-**2005**[1,3]**,** Anchorage-**2002**[4]**,** Vancouver-**2000**[1], Barcelona**-1998**[1,3], San Diego-**1993**[1]**,** Toronto-**1991**[1,3]**,** Seattle-**1990**[1,3]**,** Jerusalem-**1989**[1,2,3] ,

  Member of the Program Committee[1], Publicity and Publication chair[2], Session chair[3] , Steering Committee[4]

- Member of the Israel Innovation award nomination committee, and session chair at the 1st, 2nd and 3rd Israel Innovation Summits, Haifa Israel, **April 2006**, **April 2007,** Tel Aviv **September 2009**
- Member of IEEE SIGARCH **Maurice Wilkes award nomination committee 2006 – 2009,** (committee's chair in 2007)
- **IPDPS: IEEE International Parallel & Distributed Processing Symposium**, Rodos, Greece, **April 2006, April 2007,** Architecture track Program Committee member
- **"Grand Research Challenge Revitalizing Computer Architecture Research"** symposium member **Computing Research Association (CRA) Discussions** by invitee only, Monterey, CA US, **December 5-7, 2005**
- **Associate Editor of *IEEE Computer Architecture Letters* Journal**, **2001 – present**
- **4th/ 5th/ 6th/ 7th Workshop on Media and Streaming Processors;** in conjunction with the 35th/ 36th/ 37th/ 38th International Symposium on Microarchitecture **(MICRO)**, Istanbul Turkey/San Diego, California/Portland, Oregon, Barcelona, Spain **November 2002/December 2003/December 2004/December 2005/December 2006,** Member of the Program Committee
- **The Hebrew University in Jerusalem, Israel;** "New Engineering School" curriculum and school's structure, consultant to the University President, **June, 2002 – 2005 (limited activity)**
- **Intel's 3st MicroArchitecture Forum**, Barcelona, Spain **June 2004,** program committee member and session chair
- **Intel's Student contest**, member of the judge committee**,** Bangalore, India, Innovation day, **May 4, 2004**
- Associate Editor **of *IEEEMicro*,** (Professional Journal), **1992 – 2004**
- **MICRO32 Conference;** Haifa, Israel, **November 17, 1999,** Member of the Program Committee
- **Intel's Microprocessor Product Group (MPG) Innovation day**, judge committee member, **Santa Clara, 1988**
- **Intel's** Fellow nomination committee, **1998 – 2000**
- **The Hebrew University in Jerusalem, Israel;** Member of the "New Engineering School" committee: Definition, directions and curriculum of a new "Engineering School" at the Hebrew University, **1998**
- **Israeli Council for High Education ("VATAT"), Ministry of Education;** Member of the approval committee for a "College Status" to HADASA School, **1997-1998**
- **Israeli Start-Up Incubator, Haifa, MATAM;** Member of the approval committee, **1997-1998**
- **International MASCOTS Conference;** Israel, **January 1997,** Member of the Technical Committee
- **IPACT96;** Boston, **October 1996,** Member of the Technical Committee
- **IEEE Computer Society, Computing Week;** Israel, **November 1994** Session Chairman of "VLSI day"
- **Hot Chips IV Symposium;** Stanford, **August 1992** Member of the Technical Committee, Session chairman
- **Intel Design Technology Conference (IDTC);** Folsom **1991,** Chairman of the Architecture Track
- **CompEuro 90 International Computer Conference;** Israel, **1990,** Member of the Program Committee
- **The 5th Jerusalem Conference for Information Technology;** Israel, **1990,** Panel member and presentation in VLSI Workshop "CISC Micro Architecture Roadmap"
- **IEEE Conference;** Israel, **April 1987, April 1989,** Session Chairman of VLSI and CAD session and a member of the Technical Committee
- **International Conference on Computer Design (ICCD);** N.Y., **October 1988, October 1989,** member of Technical Program Committee, Architecture and Algorithms Track and MicroProcessor Architecture Sessions chairman.

PUBLICATIONS

Theses:

- **U. C. Weiser**
  "Mathematical and Graphical Tool for the Creation of Computational Arrays". **Ph.D Thesis,** August **1981**, University of Utah, SLC, UT
- **U. C. Weiser**
  "A Logarithmic Preamplifier for Laser Signal Detecting", **M.Sc Thesis,** March **1975**, Technion IIT, Haifa, Israel.

Books, Reviewed Professional Journals, Reviewed Conferences:

- **Z. Guz, I. Keidar, A. Kolodny, U. Weiser**
  "Caches vs. Threads; Multicore vs. Multithread machines" CCIT, EE Technion Technical Report (?)
- **E. Rotem, R. Genosar, A. Medelson, U. Weiser**
  "Multiple Clock and Voltage Domains for Chip Multi Processors" MICRO 2009 conference, NY, NY December 12th 2009
- **A. Berman, U. Weiser**
  "Reliable Architecture for Flash Memory", Workshop on Emerging Memory Technologies (WEMT) 2009 held in conjunction with ISCA-36 Austin, Texas, June, 2009
- **Z. Guz, E. Bolotin, I. Keidar, A. Kolodny, A. Mendelson, U. Weiser**
  "Multi-Core vs. Multi-thread Machines: Stay away from the valley" IEEE Computer Architecture Letters **Journal**, IEEE Publication, April 2009
- **T. Morad, A. Kolodny, U. Weiser**
  "Multiple Multithreaded Applications on Asymmetric and Symmetric Chip MultiProcessors"
  CCIT (EE Technion) technical report #701, August 2008
- **Z. Guz, I. Keidar, A. Kolodny, U. Weiser**
  "**Utilizing Shared Data in Chip Multiprocessors with the Nahalal Architecture"** SPAA, 20th ACM Symposium on Parallelism in Algorithms and Architectures, Munich, Germany, June 14-16, 2008. Won **SPAA 2008 Conference**'s best paper award
- **A. Elyada, R. Ginosar, U. Weiser "Low-Complexity Policies for Energy-Performance Tradeoff" IEEE Transactions on Very Large Scale Integration Systems Journal to be published July 2008**
- **G. Amit, Y. Caspi, R. Vitale, U. Weiser, A. Pinhas**
  "Scalability of Multimedia Applications on Next-Generation Processors" ICME 2006 Conference, Toronto, July 9 - 12, 2006
- Z**. Guz, I. Keidar, A. Kolodny, U. Weiser**
  "Nahalal: Cache Organization for Chip Multiprocessors" IEEE Computer Architecture Letters **Journal**, IEEE Publication, June 2007 also Technion Technical Report: CCIT 600, September 2006
- **T. Morad, U. Weiser, A. Kolodny, M. Valero, E. Ayguade**
  "Performance, Power Efficiency and Scalability of Asymmetric Cluster Chip MultiProcessors"
  Computer Architecture Letter **Journal**, IEEE Publication, July 2005
- **T. Morad, U. Weiser, A. Kolodny**
  "Why NOT Data Trace Cache", WDDD 2005, Fourth Annual **Workshop** on Duplicating, Deconstructing and Debunking (Held in conjunction with ISCA32), Madison Wisconsin, June 4th, 2005
- **T. Morad, U. Weiser, A. Kolodny**
  "ACCMP - Asymmetric Cluster Chip Multiprocessing", EE Technion, **Technical Report** CCIT Report #488, **June 2004**
- **N. Magen, A. Kolodny, U. Weiser, N. Shamir**
  "Interconnect - Power Dissipation in a Microprocessor", IEEE SLIP2004 (System Level Interconnect Predication) **Conference,** Paris, **February 2004**
- **M. Bekerman, S. Jourdan, R. Ronen, G. Kirshenboim, L. Rappoport, A. Yoaz, U. Weiser**
  "Correlated Load - Address Predictors", ISCA-26 Conference, Atlanta, May 1999
- **U. Weiser et al**
  "The Complete Guide to MMX™ Technology", McGraw-Hill Book, (313 pages book, 9 authors), June 1997

- **M. Mittal, A. Peleg, U. Weiser**
  "**MMX Technology Architecture Overview**", Intel Technology Journal, September 1997
- **A. Peleg , S. Wilkie, U. Weiser**
  "Intel MMX for Multimedia PCs", Communication of the ACM Journal, Vol 40, Number 1, p25-38, January **1997**
- **A. Peleg, U. Weiser**
  "MMX Technology Extension to Intel Architecture", IEEEMicro Journal, pp. 42-50, August 1996
- **A. Peleg, U. Weiser, et al**
  "The MMX Technology Extension to the Intel Architecture", Intel Design Technology Conference (DTTC), Tucson, Arizona, June 1996
- **U. Weiser**
  "Tradeoff considerations and performance of Intel's MMX Technology", Hot Chips Symposium, Stanford, California, August 19, 1996
- **U. Weiser, et al**
  "Intel's Multimedia Architecture Extension", The 19th Convention of Electrical and Electronics Engineering in Israel, Jerusalem, Israel, November 5, 1996
- **A. Peleg, U. Weiser; "Dynamic Flow Instruction Cache Memory Organized Around Trace Segments Independent of Virtual Address Line",** United States Patent No. 5,381,533, Jan 10, 1995 (*aka Trace Cache Patent (also in the patent list)*
- **F. Klass, U. Weiser**
  "Efficient Systolic Array for Matrix Multiplication", proceedings of 1991 International Conference on Parallel Processing", (ICPP) Boca Raton, FL, August 1991
- **A. Peleg, U. Weiser**
  "Future Trends in MicroProcessors: Out of Order Execution, Speculative Branching and their CISC Performance Potential", proceedings of IEEE Conference, Tel-Aviv, Israel, March 1991
- **U. Weiser, Y Yaari, A. Golbert, S. Rotem et al**
  "Intel's P_X next generation Microprocessor" Intel internal confidential document (the initial definition of the Pentium Processor), January 1991
- **U. Weiser, Y. Yaari**
  "CISC Superscalar Processor", Intel Design Technology Conference, Gleneden Beach, Oregon, June 1990
- **U. Weiser, D. Perlmutter, Y. Yaari**
  "Reducing the Cost of Branches for CISC MicroProcessors", Intel Design Technology Conference, June 1989
- **D. Alpert, D. Biran, L. Epstein, J. Levy, B. Maytal, Y. Sidi, U. Weiser**
  "Trends in VLSI Microcomputer Design", proceedings of International Conference on Computer Technology, System and Application (CompEuro-87), pp. 564-567, May 1987
- **U. Weiser, Y. Sidi, L. Epstein, D. Biran, A. Kaminker**
  "Design of the NS32532 MicroProcessor", 1987 IEEE International Conference on Computer Design (ICCD): VLSI in computers and Processors, pp. 177-180, October 1987
- **Y. Sidi, D. Alpert, D. Biran, L. Epstein, J. Levy, B. Maytal, U. Weiser**
  "Design Consideration of an Advanced 32-bit MicroProcessor", proceedings of IEEE Conference, TA, Israel, April 1987
- **Y. Rimoni, I. Zisman, R. Genosar, U. Weiser**
  "Communication Element for the Versatile MultiComputer", proceedings of IEEE Conference, TA, Israel, April 1987
- **U. Weiser, A.L. Davis**
  "Wavefront Notation Tool for VLSI Array Design", in VLSI System and Computation, H.T. Kung, R.F. Sproull, G.T. Steele Book Editors, Computer Science Press Inc., pp. 226-234, 1981
- **L. Johnson, U. Weiser, D. Cohen, A.L. Davis**
  "**Towards a Formal Treatment of VLSI Arrays**" proceedings of Caltech Conference on VLSI, January 1981
- **U. Weiser, A. L. Davis**
  "Mathematical Representation for VLSI Arrays", Univ. of Utah Tech. Report, UUCS-80-111, Sept. 1980
- **U. Weiser, A. F. Arbel, A. Adin**
  "**Speed Limitation of Feedback Amplifiers due to Signal Delay**", International Journal of Electronics Journal, Vol. 41, September 1975

- **U. Weiser, A. F. Arbel, A. Adin**
  "Analysis of Feedback Amplifiers considering the Amplifier Delay", proceedings of IEEE Conference, Tel-Aviv, Israel, April 1975

Major Technical Achievements :

1. Analytical model of a fast feedback amplifier with delay *(1975)* (Master thesis)
2. Mathematical and graphical model of Systolic Arrays *(1981)* (Ph.D thesis)
3. Initiation, definition and architecture simulator of Intel's first Pentium Processor *(1988)*
4. Invention (with Alex Peleg) of the Trace cache *(1989)*
5. Performance analysis and potential of X86 Out of Order machine (with Peleg) *(1990)*
6. Leading the Intel's MMX technology *(1996)*
7. Leading at Intel the Asymmetric Media Architecture Initiative (failed at Intel) *(2002)* (confidential material)
8. Content Aware Action concept (with Horowitz, Ganor, Shachar, Cohen @ Commex-Technologies) *(2007)*
9. Nahalal – Cache organization for Chip MultiProcessor (with Guz, Keidar and Kolodny) *(2008)*
10. Multi-Core vs. Multi-Thread Machines (with Guz, Bolotin, Keidar, Mendelson and Kolodny) *(2009)*